REMARKS

Applicant has carefully reviewed and considered the official action and the references cited therein. Claims 1, 4, 6, and 13 have been amended for clarity. Support for all amended claims can be found in the specification, and no new matter has been added by these amendments. Reconsideration and withdrawal of the rejections are respectfully requested in view of the foregoing amendment and following remarks.

CLAIM REJECTIONS

Claim Rejections-35 U.S.C. §112

Claims 1-14 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, the examiner asserted that the original specification does not support and describe the claimed limitations of "performing a second ion implantation into the semiconductor substrate of the active region under the gate oxide layer to compensation for an ion concentration...". The examiner further stated that since just a gate oxide film is formed on the semiconductor substrate, during the ion implanting step, the ions would be thereby implanted into the whole active region A under that thin gate oxide film.

Claims 1 and 6, as amended, recite that the second ion implantation is carried out into the semiconductor substrate of the active region beside the trench and vertically overlapped with the polysilicon film. It is believed the claims, as amended, are fully described in the specification.

Accordingly, the applicants respectfully submit that amended claims 1 and 6 comply with §112, paragraph 1, such that the rejection is overcome. Reconsideration and withdrawal of the rejection are respectfully solicited.

Claim Rejections-35 U.S.C. §102/103

Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated, or in the alternative under 35 U.S.C. 103(a), by Wu (2002/0115270) in view of Oda et al (US. 2002/0086498).

Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner (US. 5,985743) taken with Oda et al (US. 2002/0086498).

Claims 6 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu (2002/0115270) and Oda et al (US. 2002/0086498), as applied to claims 1 and 5 above, taken with Sung (US. 5,550,078).

Applicants traverse the rejections for the following reasons.

Amended independent claim 1 recites a method of forming a device isolation film in a semiconductor device, comprising of: performing a first ion implantation process for controlling a threshold voltage in an active region of a semiconductor substrate; sequentially forming a gate oxide film and a polysilicon film over the semiconductor substrate; forming a trench having a side wall to define the active region and an isolation region by etching a portion of the polysilicon film, the gate oxide film, and the semiconductor substrate; forming a side wall oxide film within the trench by performing an oxidation process; performing a second ion implantation process into the semiconductor substrate of the active region beside the trench and vertically overlapped with the polysilicon film to compensate for a concentration of ions implanted for controlling the threshold voltage; and forming an isolation structure by filling an oxide film inside the trench.

Amended independent claim 6 recites a method of forming a device isolation film in a semiconductor device, comprising forming a screen oxide film on the semiconductor substrate; performing a first ion implantation process for controlling a threshold voltage in an active region of a semiconductor substrate; removing the screen oxide film; sequentially forming a gate oxide film, a polysilicon film, and a pad nitride film on the semiconductor substrate; forming a trench to define the active region and an isolation region by sequentially etching a portion of the pad

nitride film, the polysilicon film, the gate oxide film, and the semiconductor substrate; forming a side wall oxide film within the trench by performing an oxidation process; performing a second ion implantation process into the semiconductor substrate of the active region beside the trench and vertically overlapped with the polysilicon film to compensate for a concentration of ions implanted for controlling the threshold voltage; removing the pad nitride film; and forming an isolation structure by filling an oxide film inside the trench.

Both claims 1 and 6 recite performing a first ion implantation process for controlling a threshold voltage in an active region of a semiconductor substrate and performing a second ion implantation process into the semiconductor substrate of the active region beside the trench and vertically overlapped with the polysilicon film to compensate for a concentration of ions implanted for controlling the threshold voltage.

Wu, Oda, Gardner, and Sung fail to teach or describe features of the amended claims 1 and 6. Particularly, Wu, Oda, Gardner and Sung fail to teach or describe a step of performing a second ion implantation process into the semiconductor substrate of the active region beside the trench and vertically overlapped with the polysilicon film to compensate for a concentration of ions implanted for controlling the threshold voltage of the amended claims 1 and 6.

Referring to Wu, there is no polysilicon layer during the ion implantation. Likewise, there is a spacer 104a. Thus, the field-encroachment implantation without affecting the active area (Col. 2, paragraph 0016) is performed into the trench surface regions to form the implanted regions 102b/200b and the surface regions 102c/200c as shown in Figs. 2A, 2B, 3D. As depicted in Figs. 2A, 2B, the implanted regions 102b/200b and the surface regions 102c/200 are not formed an area vertically overlapped with a conductive layer. Therefore, an ion implantation process is performed only once into an active region beside the trench and vertically overlapped with a conductive layer.

Referring to Oda, there is also no polysilicon layer during the ion implantation. Likewise, ion implantation is performed only once into an active region beside the trench.

Referring to Gardner and Sung, only one ion implantation is performed into an area beside a trench and vertically overlapped with a conductive gate structure.

However, according to the invention, the ion implantation process is performed twice into an active region beside the trench and vertically overlapped with the polysilicon film to compensate for a concentration of ions implanted for controlling the threshold voltage. As a result, it is possible to improve the performance of the device.

Accordingly, applicant respectfully submits that claims 1 and 6 are not anticipated by, or in the alternative obvious in view of Wu, Oda, Gardner, and Sung, whether taken singly or in combination.

Claims 5 and 14, which are dependent on the base claims, are also patentable for the reasons discussed above with respect to base claims 1 and 6, as well as on their own merits.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270) or Gardner (5,985,743) taken with Oda et al (2002/0086498).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270) or Gardner (5,985,743) and Oda et al (2002/0086498), taken with Hong (6,030,882).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270) or Gardner (5,985,743) and Oda et al (2002/0086498) taken with Oda et al. (2002/0086498).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270) and Oda et al (2002/0086498), as applied to claims 1, 5 above, and Sung (5,550,078) as applied to claim 6 above.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270), Oda et al (2002/0086498), and Sung (5,550,078), as applied to claim 6 above, taken with Hong (US. 6,030882).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270), Oda et al (2002/0086498), and Sung (5,550,078) as applied to claim 6 above.

Claims 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270), and Oda et al (2002/0086498), and Sung (5,550,078) as applied to claim 6 above, and further of Houlihan (2001/0021545) or Dong (2003/0119256).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270), and Oda et al (2002/0086498), and Sung (5,550,078) as applied to claim 6 above, and further of Kim (2003/0067050) and/or Dong (2003/0119256).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270), and Oda et al (2002/0086498), and Sung (5,550,078) as applied to claim 6 above, and further of Sung et al (6,180,453) and/or Dong (2003/0119256).

The respective rejections of claims 2-4 and 7-13 as being unpatentable are respectfully traversed, as it is submitted that the recited elements of amended claims 1 and 6 are not shown in applied references, whether taken singly or in combination, and that the references provide no suggestion or motivation to supply the missing elements.

Accordingly, the examiner is respectfully requested to pass this application to issue.

Should the examiner wish to discuss the foregoing or any matter of form in an effort to advance this application toward allowance is urged to telephone the undersigned at the indicated number.

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Respectfully submitted,

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